Associate Professor دانشگاه شهید بهشتی

Electrical Engineering - Electronics and / Telecommunications

Somayyeh Timarchi

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Education

- B.Sc: SHAHID BEHESHTI UNIVERSITY, , 1377→1381
- Ph.D: SHAHID BEHESHTI UNIVERSITY, , 1383→1388
- M.Sc: Sharif University of Technology, , 1381→1383

Research Interests

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-
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Professional Experiences

- , 1400→1400
- , 1397→1398
- Technical Program Committee Member in ICECS 2018, 1396→1397
- Technical Program Committee Member in ICECS 2017, 1395→1396
- , 1394→1394
- , 1392→1394
- , 1392→1393

Journal Papers

- Non-Volatile and High-Performance Cascadable Spintronic Full-Adder with no Sensitivity to Input Scheduling
Mina Raouf, Somayyeh Timarchi
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II-EXPRESS BRIEFS, Vol.70, pp. 2236-2240, 2023

■ Two Efficient Approximate Unsigned Multipliers by Developing New Configuration for Approximate 4:2 Compressors
Ladan Sayadi, Somayyeh Timarchi, Akbar Sheikh-Akbari
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS, Vol.70, pp. 1649-1659, 2023

■ Reducing the Effect of Carry Propagation on Spintronic Adders
Mina Raouf, Somayyeh Timarchi
SPIN, Vol.12, 2022

■ Ultra-lightweight FPGA-based RC5 designs via data-dependent rotation block optimization
Yahya Arzani birgani, Somayyeh Timarchi, Ayesha Khalid
MICROPROCESSORS AND MICROSYSTEMS, Vol.93, 2022

■ Teaching redundant residue number system for electronics and computer students
Somayyeh Timarchi
International Journal of Mathematical Education in Science and Technology, Vol.-, pp. 1-19, 2022

■ Area-Time-Efficient Scalable Schoolbook Polynomial Multiplier for Lattice-Based Cryptography
Yahya Arzani birgani, Somayyeh Timarchi, Ayesha Khalid
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■ Efficient Approximate Multiplier Based on a New 1-Gate Approximate Compressor
Seyed Amir Hossein Ejtahed, Somayyeh Timarchi
CIRCUITS SYSTEMS AND SIGNAL PROCESSING, Vol.41, pp. 2699-2718, 2022

■ Sign Detection and Signed Integer Comparison for the 3-Moduli Set {2^n-1,2^(n+k),2^n+1}?
Zeinab Torabi, Somayyeh Timarchi
Computer Science, Vol.22, pp. 387-401, 2021

■ Area and Power-Efficient Variable-Sized DCT Architecture for HEVC Using Muxed-MCM Problem
Ahmad Shabani, Mohammad Sabri, Bahareh Khabbazan, Somayyeh Timarchi
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS, Vol.68, pp. 1259-1268, 2021

■ Improved Distributed Particle Filter Architecture with Novel Resampling Algorithm for Signal Tracking
Zahra Talebi, Somayyeh Timarchi
International Journal of Engineering, Vol.33, pp. 2482-2488, 2020

■ Improving Architectures of Binary Signed-Digit CORDIC With Generic/Specific Initial Angles
Hossein Mahdavi, Somayyeh Timarchi
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS, Vol.67, pp. 2297-2304, 2020

■ Efficient Error Detection and Correction Method for 1-out-of-3 Binary Signed Digit Adders
Adib Armand, Somayyeh Timarchi
INTERNATIONAL JOURNAL OF ELECTRONICS, Vol.106, pp. 1427-1440, 2019

■ Area-Time-Power Efficient Maximally Redundant Signed-Digit Modulo 2n ? 1 Adder and Multiplier
Somayyeh Timarchi, Negar Akbarzadeh Chini Foroush
CIRCUITS SYSTEMS AND SIGNAL PROCESSING, Vol.38, pp. 2138-2164, 2019

■ Area-Time-Power Efficient FFT Architectures Based on Binary-Signed-Digit CORDIC
Hossein Mahdavi, Somayyeh Timarchi
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS, Vol.66, pp. 3874-3881, 2019

■ Power and area efficient CORDIC-Based DCT using direct realization of decomposed matrix
Ahmad Shabani, Somayyeh Timarchi, Hossein Mahdavi
MICROELECTRONICS JOURNAL, Vol.91, pp. 11-21, 2019

■ Optimized Parity-Based Error Detection and Correction Methods for Residue Number System
Adib Armand, Somayyeh Timarchi, Hossein Mahdavi
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■ Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates

Hamed Naseri, Somayyeh Timarchi
IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, Vol.26, pp. 1481-1493, 2018

■ Low-Power DCT-Based Compressor for Wireless Capsule Endoscopy
Ahmad Shabani, Somayyeh Timarchi
SIGNAL PROCESSING-IMAGE COMMUNICATION, Vol.59, pp. 83-95, 2017

■ Efficient modulo 2n 1 multiplier
Masoud Abbasi Alaie, Somayyeh Timarchi
International Journal of Computer Aided Engineering and Technology, Vol.8, pp. 260-276, 2016

■ An Ultra-Low-Power 9T SRAM Cell Based on Threshold Voltage Techniques
Majid Moghaddam, Somayyeh Timarchi, Mohammad Hossein Moaiyeri, Mohammad Eshghi
CIRCUITS SYSTEMS AND SIGNAL PROCESSING, Vol.35, pp. 1437-1455, 2016

■ Fast Architecture for Decimal Digit Multiplier
Mahmood Fazlali, Hadi Valikhani, Somayyeh Timarchi, Hadi Tabatabaee Malazi
MICROPROCESSORS AND MICROSYSTEMS, Vol.39, pp. 296-301, 2015

■ Generalized Fault-Tolerant Stored-Unibit-Transfer RNS Multiplier for Moduli Set 2n-1 2n 2n 1
Somayyeh Timarchi, Mahmood Fazlali
IET Computers and Digital Techniques, Vol.6, pp. 269-276, 2012

■ Efficient Modular Binary Signed-Digit Multiplier for the moduli set 2n-1 2n 2n 1
Maryam Saremi, Somayyeh Timarchi
Journal on Computer Science and Engineering, Vol.9, pp. 52-62, 2011

■ Efficient Reverse Converter Designs for the New 4-Moduli Sets 2n 1 2n 2n 1 22n 1 1 and 2n 1 2n 1 22n 22n 1 Based on New CRTs
, Keyvan Navi, , , Somayyeh Timarchi
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■ A novel low-power full-adder cell for low voltage
Keyvan Navi, Mehrdad Maeen, Vahid Foroutan, Somayyeh Timarchi, Omid Kavehei
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■ Arithmetic Circuits of Redundant SUT-RNS
Somayyeh Timarchi, Keyvan Navi
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■ Improved Modulo 2n +1 Adder Design
Somayyeh Timarchi, Keyvan Navi
International journal of computer and information science and engineerin, Vol.2, pp. 158-165, 2008

■ برای پردازنده سیگنال دیجیتال n+۱ضرب کننده و ضرب جمع کننده پیمانه ۲
نگار اکبرزاده چینی فروش، سمیه تیمارچی
پردازش علائم و داده ها، نسخه ۳۵، صفحات: ۱۲۷-۱۳۸، ۱۳۹۶

Conference Papers

■
Mohammad ebrahim Romani, Somayyeh Timarchi
27th Iranian Conference on Electrical Engineering ICEE2019

■ Novel Algorithm and Architectures for High-Speed Low-Power ConText-Based Steganography
Somayyeh Timarchi, Masoud Abbasi Alaie, Hosein Kooshkbaghi
19th CSI International Symposium on Computer Architecture and Digital Systems (CADS17)

■ Ultra-Low Voltage Standard Cell Libraries Design Strategies and a Case Study

Somayyeh Timarchi, Massimo Alioto
The 23rd IEEE International Conference on Electronics Circuits and Systems (ICECS), pp.520-523

■
Amir Abbas Hamidi Imani, Somayyeh Timarchi, Negar Akbarzadeh Chini Foroush
1st International Conference on New Research Achievements in Electrical and Computer Engineering

■ Block-based hardware implementation of FAST corner detection algorithm
Amir Abbas Hamidi Imani, Somayyeh Timarchi, Negar Akbarzadeh Chini Foroush
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■ Maximally Redundant High-Radix Signed-Digit Residue Number System
Somayyeh Timarchi, Negar Akbarzadeh Chini Foroush, Amir Abbas Hamidi Imani
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■ High-speed energy-efficient 5 2 compressor
Ardalan Najafi, Somayyeh Timarchi, amir najafi
37th International Convention on information and communication technology electronics and microelectronics, pp.80-84

■ Efficient 1-out-of-3 Binary Signed-Digit Multiplier for the moduli set 2n-1 2n 2n 1
Maryam Saremi, Somayyeh Timarchi
17th CSI International symposium on Computer Architecture and Digital Systems (CADS2013), pp.123-124

■ High-speed binary signed-digit RNS adder with posibit and negabit encoding
Somayyeh Timarchi, Maryam Saremi, Mahmood Fazlali, Georgi Gaydadjiev
21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), pp.58-59

■ Efficient Class of Redundant Residue Number System
Somayyeh Timarchi
ISVLSI 2013, pp.10-16

■ 1-out-of-3 Binary Signed-Digit Modular Adder
Maryam Saremi, Somayyeh Timarchi
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■ A Novel High-Speed Low-Power Binary Signed-Digit Adder
Somayyeh Timarchi, Parham Ghayoor,
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■ A unified addition structure for moduli set 2n-1 2n 2n 1 based on a novel RNS representation
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■ An Efficient Power-Area-Delay Modulo 2n-1 Multiplier
Somayyeh Timarchi, Mahmood Fazlali
the 15th CSI international symposium on computer architecture and digital systems (cads), pp.157-160

■ Maximally Redundant High-Radix Signed-Digit Adder New Algorithm and Implementation
Somayyeh Timarchi, Keyvan Navi, Omid Kavehei
IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2009), pp.97-102

■ Efficient Class of Redundant Residue Number
Somayyeh Timarchi, Keyvan Navi
2007 IEEE International Symposium on Intelligent Signal Processing, pp.1-6

■ EVALUATION OF SOME EXPONENTIAL RANDOM NUMBER GENERATORS IMPLEMENTED BY FPGA
Somayyeh Timarchi, S. Ghassem Miremadi, Alireza Ejlali
The IASTED International Conference on Parallel and Distributed Computing and Networks (PDCN 2005), pp.578-583

Design and Implementation of a Low–Power FIR Filter ■
علی دهقانی فیروزآبادی، سمیه تیمارچی، کیاوش قمصری
دومین کنفرانس میکروالکترونیک ایران

■ بهبود توان مصرفی ضرب کننده ی غیر علامت دار تقریبی با قابلیت بازیابی خطای قابل تنظیم

لادن صیادی، سمیه تیمارچی

بیست و هشتمین کنفرانس مهندسی برق ایران، صفحات: ۱-۵

■ Power Investigation of ۴-۲ Compressors by Changing Input Switching Activity

امیرمحمد کتابچی، سمیه تیمارچی

اولین کنفرانس میکروالکترونیک ایران، صفحات: ۱-۴

■ برای کاربردهای با منابع سخت افزاری محدود و نرخ داده متوسط RC۶ پیاده سازی الگوریتم

یحیی ارزانی بیرگانی، سمیه تیمارچی

نهمین کنفرانس ملی فرماندهی و کنترل ایران

■ با مسیر داده ۸ بیتی به منظور دست یابی به سربار سخت افزاری کمینه RC۵ طراحی و پیاده سازی الگوریتم

یحیی ارزانی بیرگانی، سمیه تیمارچی

سیزدهمین کنفرانس بین المللی انجمن رمز ایران

■ Low Power Design of Binary Signed Digit Residue Number System Adder

ادیب آرمندبروجنی، سمیه تیمارچی

بیست و چهارمین کنفرانس مهندسی برق ایران

■ Efficient Multiply-add Unit Specified for DSPs Utilizing Low-Power Pipeline Modulo ۲n ۱ Multiplier

نگار اکبرزاده چینی فروش، سمیه تیمارچی، امیرعباس حمیدی ایمانی

نهمین کنفرانس ماشین بینایی و پردازش تصویر ایران

■ معماری کم مصرف برای تبدیل گسسته کسینوسی بر پایه ساختار کوردیک پیش بینی جدید

احمد شعبانی، سمیه تیمارچی

نهمین کنفرانس ماشین بینایی و پردازش تصویر ایران

■ پردازنده چند هسته ای پایگاه پردازش داده در شبکه حسگرهای بی سیم

اردوان یزدی، سمیه تیمارچی

صفحات:۳۴۶۵-۳۴۷۰، ICEE۲۰۱۴بیست و دومین کنفرانس مهندسی برق ایران

■ پیاده سازی بهینه الگوریتم های نهان نگاری با قابلیت پیکربندی مجدد

مسعود عباسی علائی، سمیه تیمارچی

صفحات:۲۵۶۳-۲۵۶۸، ICEE۲۰۱۴بیست و دومین کنفرانس مهندسی برق ایران

■ Radix-۴ Implementation of Redundant Interleaved Modular Multiplication on FPGA

لقمان رحیم زاده، محمد عشقی، سمیه تیمارچی

صفحات:۵۲۳-۵۲۶، ICEE۲۰۱۴بیست و دومین کنفرانس مهندسی برق ایران

■ A Novel Modulo ۲n+۱ Adder Scheme

سمیه تیمارچی، کیوان ناوی

دوازدهمین کنفرانس بین المللی سالانه انجمن کامپیوتر ایران ۱۳۸۵

■ RNS طراحی جدید جمع کننده چند عملوندی سریع

مهدی حسین زاده، سمیه تیمارچی، امیرپاشا میربهاء، کیوان ناوی

۱۴th Iranian Conference on Electrical Engineering ICEE۲۰۰۶

■ ۱ nبرای پیمانه ۲ RNS مقاله طراحی جدید تفریق کننده

سمیه تیمارچی، کیوان ناوی، مهدی حسین زاده

یازدهمین کنفرانس بین المللی سالانه انجمن کامپیوتر ایران ۱۳۸۴

■ طراحی جدید برای کمپرسور ۳-۴

سمیه تیمارچی، کیوان ناوی

یازدهمین کنفرانس بین المللی سالانه انجمن کامپیوتر ایران ۱۳۸۴

■ A Comparative Evaluation of Some Hardware-Based Pseudo-Random Number Generators

سمیه تیمارچی، سید قاسم میرعمادی، علیرضا اجلالی

دهمین کنفرانس سالانه انجمن کامپیوتر ایران ۱۳۸۳، صفحات:۱۷-۲۵

thesis and doctoral thesis

■ Non-volatile Full-Adder Based on Magnetic Tunnel Junction
Mina Raouf
2023

■ Optimal transistor sizing for designing the low-power digital circuits
Hamed Naseri
2022

M.Sc. Theses

■ Hardware Design and Implementation of ResNet architecture Using Deep Learning Algorithms
Sadjad Asadi
2021

■ improving approximate multiplier with resource reduction approach
Ladan Sayadi
2021

■ Approximate adder design with resource reduction approach
Maryam Salimi akin abad
2021

■ A low - power design of a voltage level- shifter based on wilson current mirror
Sepideh Najafinia
2021

■ improving elliptic curve cryptography point multiplication architecture over finite field
Nima Yahyavi
2020

■ Three -Valued Memory Based on Nanoscale Spintronic Technology
Masoumeh Aliniya
2020

■
Ladan Mohebbi
2020

■ Designing and improving fault tolerant binary sign digit adder
Alireza Faraji
2020

■ Improving the efficiency of Residue Number System Scaler
Mohammad ebrahim Romani
2020

■
Ali Dehghani Firouzabadi
2019

■
Sama Hashemi
2019

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Hosein Kooshkbaghi
2019

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Mohammad Zeynali
2018

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Javad Bakhshi
2018

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Ehsan Panahifar
2018

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Hossein Mahdavi
2017

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Adib Armand
2017

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Fahimeh Abdisiahbidi
2017

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Amir Abbas Hamidi Imani
2016

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Ahmad Shabani
2016

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Negar Akbarzadeh Chini Foroush
2016

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Zahra Talebi
2016

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Milad Kamran Kashtiban
2015

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Yahya Arzani Birgani
2015

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Morteza Derakhshanzadeh
2015

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Masoud Abbasi Alaie
2014

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Maryam Saremi
2013

■
Mohammad Nobakht Motlagh Ghochani
2012